



Wed, 19 Dec 2007, 5:10:27 PM EST

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- [#9](#) ((prohibite execution from sharedmemory)<IN>metadata)
- [#10](#) execute task- cache
- [#11](#) restrict execution from ram
- [#12](#) ((restrict execution from memory)<IN>metadata)
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- [#14](#) ((restrict task execution from memory )<in>metadata)
- [#15](#) ((refusetask execution from memory )<in>metadata)
- [#16](#) ((refuse task execution from memory )<in>metadata)
- [#17](#) ( ((prohibit)<in>metadata ) <and> ((task execution)<in>metadata ) )<and> ((memory)<in>metadata )


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[N Jouppi](#)
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... external **cache access** on an internal **cache** hit, and reissues the **access** over a **main memory** bus on an ... - all 3 versions »

PG Lee, E Riggs, G Singh, R Steck - US Patent 5,345,576, 1994 - Google Patents

... TO AN INTERNAL **CACHE**, CANCELS THE EXTERNAL **CACHE ACCESS** ON AN INTERNAL **CACHE HIT**,

AND REISSUES THE **ACCESS** OVER A **MAIN MEMORY** BUS ON AN EXTERNAL **CACHE** MISS [75 ...

Cited by 32 - [Related Articles](#) - [Web Search](#)

**Making B+-trees cache conscious in main memory** - all 10 versions »

J Rao, KA Ross - ACM SIGMOD Record, 2000 - portal.acm.org

... The traditional assumption that **memory** references have uniform cost is no longer valid given the current speed gap between **cache access** and **main memory access**. ...

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**Cache Conscious Indexing for Decision-Support in Main Memory** - all 12 versions »

J Rao, KA Ross - Proceedings of the 25th VLDB, 1999 - cs.columbia.edu

... In a **main-memory** database there are several factors ... binary search), and hence relatively

few **cache** misses ... When range queries or sequential **access** are needed on ...

Cited by 113 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

**Main memory access in a microprocessor system with a cache memory** - all 3 versions »

AM Olson, TN Robinson, B Rajaram - US Patent 4,847,758, 1989 - Google Patents

... Page 5. 1 24,847,758 number of bytes actually read into the **cache memory MAIN MEMORY**

**ACCESS** IN A during the update process. Since this update of the ...

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**Scratchpad memory: design alternative for cache on-chip memory in embedded systems** - all 13 versions »

R Banakar, S Steinke, BS Lee, M Balakrishnan, P ... - Proceedings of the tenth international symposium on Hardware ..., 2002 - portal.acm.org

... 75 Page 4. **Access** Number of cycles **Cache** Using Table 2 Scratch pad 1 cycle **Main Memory** 16 bit 1 cycle + 1 wait state **Main Memory** 32 bit 1 cycle + 3 wait states ...

Cited by 120 - [Related Articles](#) - [Web Search](#)

**Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and ...** - all 38 versions »

NP Jouppi - way - portal.acm.org

... The relatively large **access** time for **main memory** in turn requires that second-level **cache** line sizes of 128 or 256B are needed. ...

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